Application Note 373
Interleaved Bus Operation
Hardware and Software Configuration

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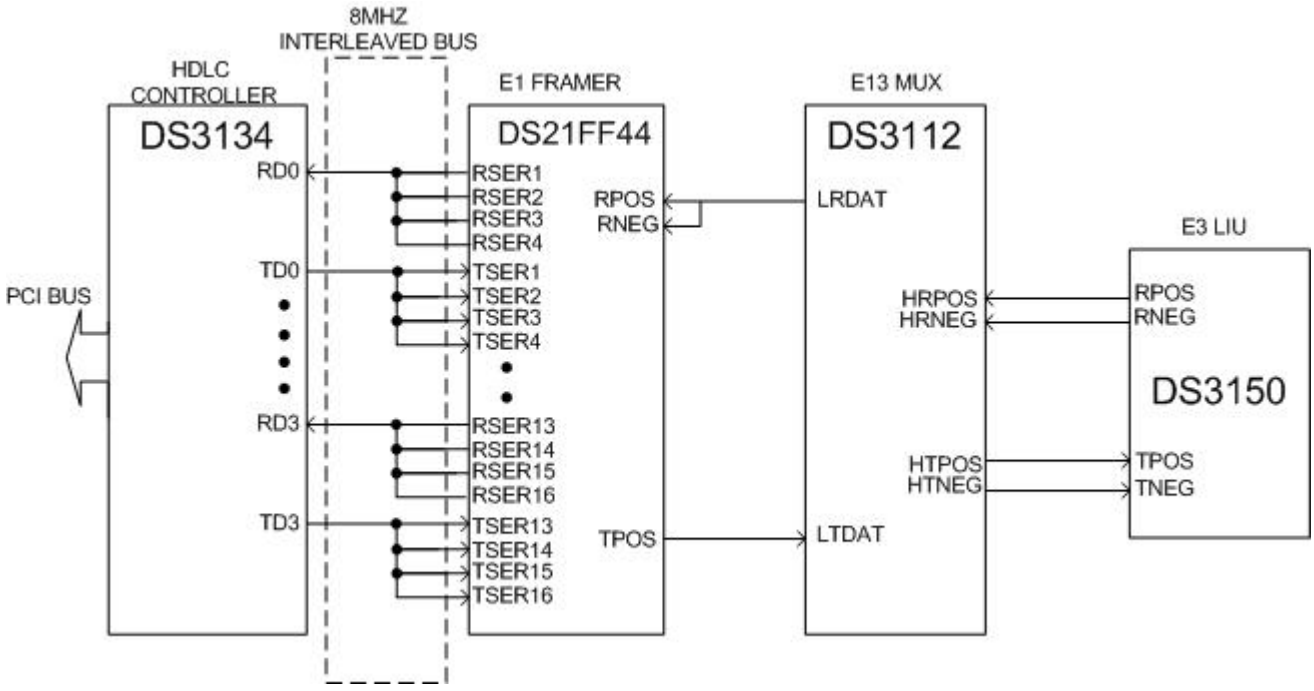
OVERVIEW

This application note describes how to configure a DS21FF44 for Interleaved Bus Operation (IBO). Focusing on the E1 framer, the application note shows applications for other E1 framers and T1 framers (DS21Q44, DS21Q42, DS21FF42/FT42) and transceivers (DS21354/52, DS21554/52, DS21Q354/Q554/Q352/Q552). The hardware connections will be identical on a T1 framer. This application note is an example of an 8.192MHz interleaved bus in byte mode.

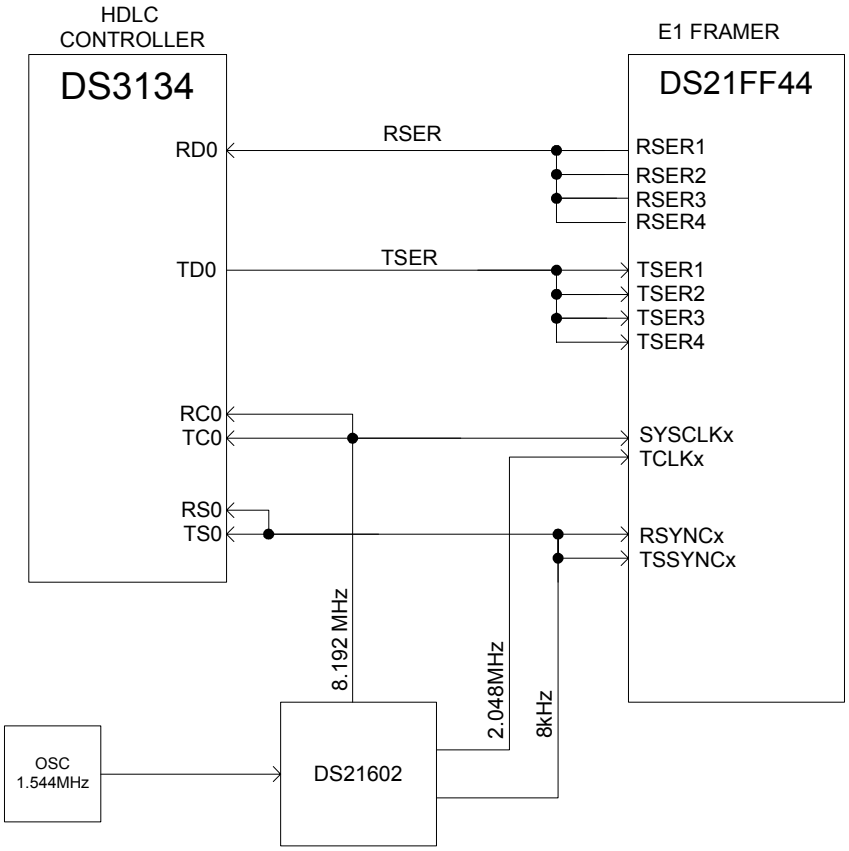
EXAMPLE OF A TYPICAL APPLICATION Figure 1



HARDWARE

Figure 2 illustrates a normal configuration of hardware connections. If the application requires frame interleaving, then TCLK and RCLK must be frequency-locked to TSYSCLK and RSYSCLK (i.e., frame slips cannot occur). Frame slips are acceptable in byte-interleaved applications. Also, RSYNC and TSSYNC must be tied together (in IBO mode, the receiver is not independent of the transmitter). The sync pulse must be phase-locked to the 8.192MHz clock as shown in Figure 3. The only difference in hardware for a T1 framer is the use of a 1.544MHz clock to connect to TCLK/RCLK rather than an E1 frequency clock. Also, in T1, every fourth channel is unused and forced to 0xFF. Consult the IBO section in the T1 data sheet for details.

CONNECTIONS FOR IBO MODE Figure 2



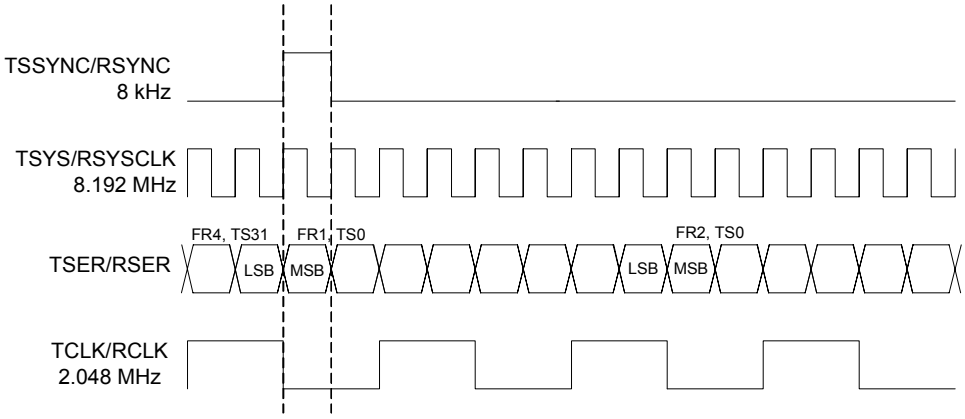
SOFTWARE

For IBO to work, the chip must be configured for IBO functionality. This includes setting the IBO register, enabling the elastic stores, and correctly configuring TSYNC and RSYNC. Additionally, users must select the 2.048MHz mode for the system clocks (both T1 and E1 framers).

The following bits must be set on all 16 framers:

E1 FRAMER	**T1 FRAMER**	
RCR1.5 = 1	RCR2.3 = 1	// Rsync is an input
RCR2.1 = 1	CCR1.2 = 1	// Receive ES enabled
RCR2.2 = 1	CCR1.3 = 1	// RSYSCLK is 2.048MHz/4.096MHz/8.192MHz
TCR1.0 = 1	TCR2.2 = 1	// TSYNC is an output
CCR3.1 = 1	CCR1.4 = 1	// TSYSCLK is 2.048MHz/4.096MHz/8.192MHz
CCR3.7 = 1	CCR1.7 = 1	// Transmit ES enabled
IBO = 0x09	IBO = 0x09	// IBO enabled, byte mode, master devices (framers 1, 5, 9, 13)
IBO = 0x08	IBO = 0x08	// IBO enabled, byte mode, slave devices (framers 2–4, 6–8, 10–12, 14–16)

TIMING DIAGRAMS FOR IBO MODE Figure 3



NOTE: TCLK/RCLK ARE FREQUENCY LOCKED BUT NOT NECESSARILY PHASE LOCKED TO THE SYSCLKS
T1 FRAMER: TCLK/RCLK = 1.544 MHz

Refer to Section 22 of the DS21FF44 data sheet for additional timing diagrams. More information about the IBO can be found in Section 20 of the data sheet.